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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/560,488

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EXAMINER

SANDVIK, BENJAMIN P

ART UNIT

PAPER NUMBER

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

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<b>Office Action Summary</b>	Application No. 10/560,488	Applicant(s) LUCOVSKY ET AL.	
	Examiner Ben P. Sandvik	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 July 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) 21-32 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☒ Claim(s) 8 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>5/9/2006</u> . | 6) <input type="checkbox"/> Other: _____  |

**DETAILED ACTION**

***Election/Restrictions***

Applicant's election without traverse of claims 1-20 in the reply filed on 7/9/2007 is acknowledged.

***Claim Objections***

Claim 8 is objected to because of the following informalities: the word "gadolinium" is misspelled. Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 4, 6-9, 14, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura et al (U.S. Patent #6097058).

With respect to **claim 1**, Nakamura teaches a semiconductor substrate (Fig. 12A, Si); a first oxide layer on the semiconductor substrate (Fig. 12A, 42 silicon dioxide), the first oxide layer comprising an element from the substrate (silicon); a second oxide layer on the first oxide layer (Fig. 12A, 44) having an ABO formula wherein A is an element of the lanthanide rare earth elements of the periodic table or the trivalent elements from cerium to lutetium; and B is an

element of the transition metal elements of groups IIIB, IVB or VB of the periodic table (Col 9 Ln 5-7).

With respect to **claims 3 and 4**, Nakamura teaches that the second oxide layer (has a band gap greater than about 5.5 eV, and a conduction band offset energy of greater than 1.5 eV (for example,  $\text{Gd}_2\text{Ti}_2\text{O}_7$  has these properties)

With respect to **claim 6**, Nakamura teaches that B is an element with 3d, 4d or 5d electrons available for bonding to oxygen (property of titanium), and wherein A is an element in which one 5d electron is available for bonding (property of lanthanides).

With respect to **claim 7**, Nakamura teaches titanium.

With respect to **claim 8**, Nakamura teaches gadolinium.

With respect to **claim 9**, Nakamura teach that the B is titanium and that A is samarium (Col 9 Ln 6).

With respect to **claim 14**, Nakamura teach that the substrate formed of silicon.

With respect to **claim 18**, Nakamura teaches that the device is field effect transistor (Col 3 Ln 61).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, in view of Hofmann et al (U.S. Patent #5606190).

With respect to **claim 2**, Nakamura does not teach that the second oxide layer has a thickness of less than 15 nm. Hofmann teaches an ABO oxide with a thickness of less than 15 nm (Col 7 Ln 1-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the second oxide of Nakamura with a thickness of less than 15 nm as taught by Hofmann in order to achieve the predictable result of functioning as a gate insulating layer.

With respect to **claim 15**, Nakamura does not teach that the substrate is an SOI substrate. Hofmann teaches an SOI substrate (Col 2 Ln 49-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Nakamura with an SOI substrate as taught by Hofmann because neighboring circuit structures can be easily isolated from one another.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, in view of Ahn et al (U.S. PG Pub #2003/0045060).

With respect to **claim 5**, Nakamura does not teach that the second oxide has an equivalent oxide thickness of about 0.5 to 1.6 nm. Ahn teaches gate oxides formed with equivalent oxide thicknesses of less than 2 nm (Paragraph 37). It would have been obvious to one of ordinary skill in the art at the time the

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invention was made to form the second oxide of Nakamura with an EOT of 0.5 to 1.6 nm based on the teachings of Ahn in order to make the oxide more uniform and easier to process.

Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, in view of Umemoto et al (U.S. Patent #5132752).

With respect to **claims 10-12**, Nakamura does not teach that the substrate comprises a Group III-V binary alloy, a Group III- V quaternary alloy, a Group III-nitride alloy, and combinations thereof. Umemoto teaches a substrate for a FET comprising InGaAs or InGaAsP (Col 10 Ln 23-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the substrate of Nakamura of InGaAs or InGaAsP as taught by Umemoto to suppress the carrier multiplication effect in the device.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, in view of Takahashi et al (U.S. Patent #6207976).

With respect to **claim 13**, Nakamura does not teach that the substrate comprises a Group III-nitride alloy selected from the group consisting of (Ga,Al)N, (Ga, In)N, (Al,In)N, (Ga,Al,In)N, and combinations thereof. Takahashi teaches a substrate for a FET comprising InGaN (Col 8 Ln 38-43). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the substrate of Nakamura of InGaN as by Takahashi in order to achieve

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the predictable result of a substrate with a suitable conductivity for semiconducting functions.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, in view of Gardner et al (U.S. Patent #5885877).

With respect to **claim 16**, Nakamura does not teach that the first oxide layer is a nitrided silicon dioxide. Gardner teaches providing a nitrided silicon dioxide as a gate dielectric (Col 4 Ln 42-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a nitrided silicon dioxide as the first insulating layer of Nakamura as taught by Gardner in order to achieve the predictable result of insulating the second oxide from the substrate.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, in view of Gardner et al (U.S. Patent #6140167).

With respect to **claim 17**, Nakamura does not teach that the first oxide layer contributes less than about 0.5 nm of oxide-equivalent capacitance to the FET. Gardner teaches a gate dielectric having an oxide-equivalent capacitance of less than about 0.5 nm (Col 9 Ln 20-24). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first oxide with an equivalent capacitance thickness as taught by Gardner in order to allow for a greater actual thickness of the oxide.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, in view of Cantarini et al (U.S. PG Pub #2001/0013627).

With respect to **claim 19**, Nakamura does not teach that the device comprises a photovoltaic device. Cantarini teaches a MOSFET device that comprises a photovoltaic device (Paragraph 13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a photovoltaic device with the device of Nakamura as taught by Cantarini in order to provide a "turn-on" signal for the MOSFET.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, in view of Schmitz et al (U.S. PG Pub #2001/0028100).

With respect to **claim 20**, Nakamura does not teach that the device comprises a high electron mobility transistor. Schmitz teaches high electron mobility transistor (Paragraph 5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the transistor of Nakamura a HEMT transistor as taught by Schmitz in order to utilize the transistor in high-power devices.

### ***Conclusion***



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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

bps

  
**EVAN PERT**  
**PRIMARY EXAMINER**